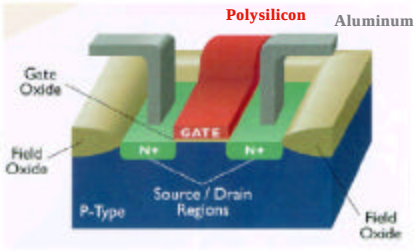
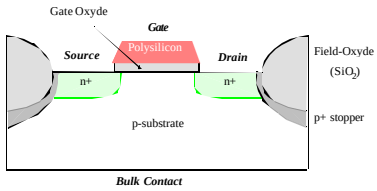
The Devices:
MOS Transistor

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

The MOS Transistor

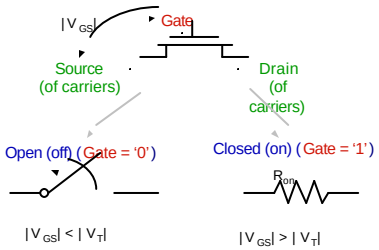


The MOS Transistor

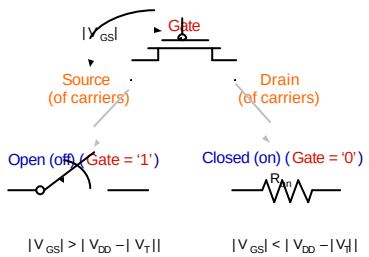


CROSS-SECTION of NMOS Transistor

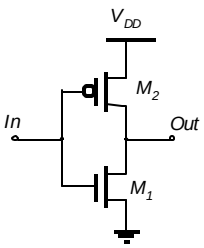
Switch Model of NMOS Transistor



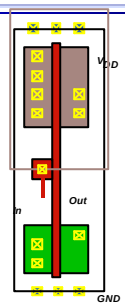
Switch Model of PMOS Transistor



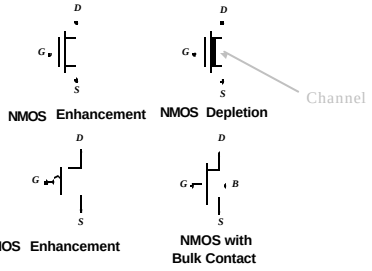
CMOS Inverter



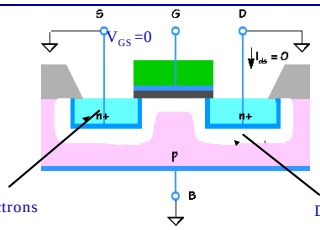
Prefered layout with minimal diffusion routing



MOS transistors Symbols



MOSFET Static Behavior

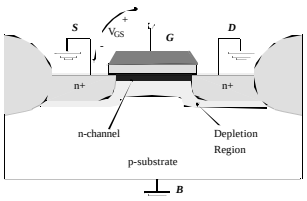


With drain and source grounded, and V_{GS} = 0, both back-to-back (sub-source, sub-drain) junctions have 0V bias and are OFF

MOSFET Static Behavior

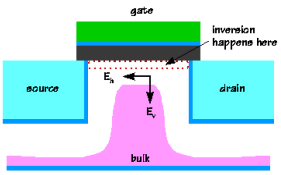
Positive voltage applied to the gate (V_{GS} > 0)

- The gate and substrate form the plates of a *capacitor.*
- Negative charges accumulate on the substrate side (repels mobile holes)
- A depletion region is formed under the gate (like *pn* junction diode)



Inversion

As the V_{GS} increases, the surface under the gate undergoes *inversion* to *n-type* material. This is the beginning of a phenomenon called *strong inversion.*



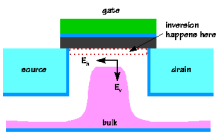
Further increases in V_{GS} do not change the width of the depletion layer, but result in more electrons in the thin inversion layer, producing a continuous *channel* from source to drain

The Threshold Voltage

The value of V_{GS} where strong inversion occurs is called the *Threshold Voltage, V_T*, and has several components:

- The flat-band voltage, V_{FB}, is the built-in voltage offset across the MOS structure and depends on fixed charge and implanted impurities charge on the oxide-silicon interface
- V_B represents the voltage drop across the depletion layer at inversion and equals to minus twice the Fermi potential ~(0.6V)
- V_{ox} represents the potential drop across the gate oxide

$$V_T = V_{FB} + V_B + V_{ox}$$



The Threshold Voltage

Where:

f_F is the *Fermi potential* (~ -0.3V for p-type substrates

Cox is the gate oxide capacitance

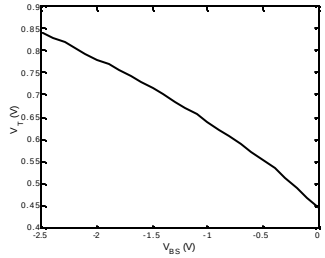
V_{SB} is the substrate bias voltage

V_{T0} is V_T at V_{SB} = 0

Note:

V_T is *positive for NMOS* transistors and *negative for PMOS*

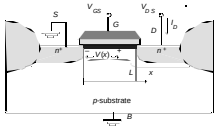
The Body Effect



Current-Voltage Relations

Assume $V_{GS} > V_T$

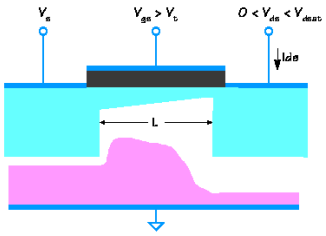
- A voltage difference V_{DS} will cause I_D to flow from drain to source
- At a point x along the channel, the voltage is V(x), and the gate-to-channel voltage is V_{GS} - V(x)
- For channel to be present from drain to source, V_{GS} - V(x) > V_T, i.e. V_{GS} - V_{DS} > V_T for channel to exist from drain to source



MOS transistor and its bias conditions

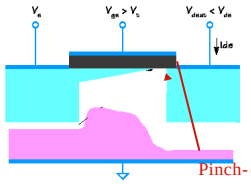
Linear (triode) Region

- When V_{GS} - V_{DS} > V_T, the channel exists from drain to source
- Transistor behaves like voltage controlled resistor



Saturation Region

- When V_{GS} - V_{DS} ≤ V_T, the channel is *pinched off*
- Electrons are injected into depletion region and accelerated towards drain by electric field
- Transistor behaves like voltage-controlled current source



Current-Voltage Relations Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = K_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

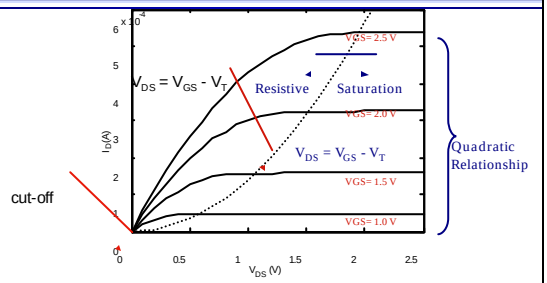
$$K_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$ Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

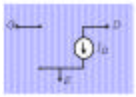
$$I_D = \frac{K_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Current-Voltage Relations Long Channel transistor



NMOS transistor, 0.25um, L_d = 10um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n W}{2\ L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$V_T = V_{T0} + \gamma\left(\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F}\right)$$

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{dsat} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1